WE CLAIM:

1. An apparatus for processing a substrate comprising a frontside and a backside used in the fabrication of an integrated device, the apparatus comprising a reaction chamber, a first load platform, and a second load platform, wherein:

the first load platform and the second load platform are disposed within the reaction chamber;

the first load platform is configured to permit a process gas to contact both the frontside and backside of a substrate loaded on the first load platform; and

the first load platform is mounted outside of the second load platform.

2. The apparatus of claim 1, wherein the first load platform is higher than the second load platform.

3. The apparatus of claim 2, wherein the first load platform is substantially directly above the second load platform.

4. The apparatus of claim 2, wherein the first load platform is at least about 10 mm higher than the second load platform.

5. The apparatus of claim 1, wherein the first load platform comprises a plurality of support pins.

6. The apparatus of claim 5, wherein the first load platform comprises three support pins.

7. The apparatus of claim 5, wherein the support pins are made from a material selected from the group consisting of quartz, silicon carbide, and silicon-carbide-coated graphite.

8. The apparatus of claim 1, wherein the second load platform is a susceptor.

9. The apparatus of claim 8, further comprising a heat source.

10. The apparatus of claim 8, wherein the reaction chamber is configured to deposit epitaxial silicon on a substrate loaded on the second load platform.

11. The apparatus of claim 1, further comprising a heat source.

12. A method for processing a substrate used in the fabrication of an integrated device, the method comprising:

loading the substrate comprising a frontside and a backside on a first load platform in a process chamber;

contacting the frontside and the backside of the substrate with a process gas while on the first load platform;

transferring the substrate to a second load platform in the process chamber; and

further processing the substrate on the second load platform.

13. The method of claim 12, wherein transferring the substrate to a second load platform comprises:

picking up the substrate using a transfer device;

moving the substrate clear of the upper load platform;

lowering the substrate to a predetermined height between the upper load platform and the lower load platform;

moving the substrate substantially directly above the lower load platform; and

loading the substrate onto the lower load platform.

14. The method of claim 13, wherein moving the substrate clear of the upper load platform comprises lifting the wafer from the upper load platform, retracting the wafer, and lowering the wafer to a vertical position between the upper load platform and the lower load platform.

15. The method of claim 12, wherein transferring the substrate to a second load platform comprises:

picking up the substrate using a transfer device;

positioning the upper load platform in a non-supporting configuration; and

lowering the substrate onto the lower load platform.

16. The method of claim 15, wherein positioning the upper load platform in a non-supporting configuration comprises horizontally moving support elements.

17. The method of claim 16, wherein the support elements comprise movable support pins.

18. The method of claim 17, wherein moving the support elements comprises rotating the support pins horizontally outwardly.

19. The method of claim 18, wherein rotating the support elements comprises rotating the support pins about an axis parallel to a tangent to the substrate.

20. The method of claim 17, wherein moving the support elements comprises retracting the support pins linearly with a horizontal movement component.

21. The method of claim 20, wherein retracting the pins further includes a vertical movement component.

22. The method of claim 12, wherein the substrate is a double-side polished single crystal silicon wafer.

23. The method of claim 12, wherein contacting the substrate with a process gas cleans native oxide from the frontside and the backside of the substrate.

24. The method of claim 23, wherein the process gas is a reducing gas.

25. The method of claim 23, wherein contacting further comprises heating the substrate.

26. The method of claim 12, wherein further processing comprises depositing a layer on the substrate.

27. The method of claim 26, wherein further processing comprises depositing the layer substantially only on the frontside of the substrate.

28. A method of processing a semiconductor substrate, comprising:

loading a substrate onto a first platform

performing a first process on the substrate while loaded upon the first platform, wherein the first process comprises upper and lower sides of the substrate to a first process gas;

moving the substrate from the first platform to a vertically adjacent second platform; and

performing a second process upon the substrate while on the second platform, wherein the second process comprises exposing substantially only the first side of the wafer to a second process gas.

29. The method of claim 28, wherein the first process comprises oxide reduction.

30. The method of claim 29, wherein the second process comprises epitaxial deposition.

31. The method of claim 28, wherein the first and second platforms are both within a single process chamber.

32. The method of claim 31, wherein moving the substrate comprises employing a robot arm extending from outside the process chamber.

33. The method of claim 28, wherein moving comprises horizontally moving support pins radially outwardly to allow substrate movement vertically from the first platform to the second platform.

34. The method of claim 28, wherein moving the substrate comprises at least one robotic retraction and extension while support elements defining the first platform remain fixed with respect to a position of the second platform.

35. A method of processing a semiconductor wafer comprising:

conducting a native oxide clean on the semiconductor wafer within a process chamber, wherein the oxide clean removes native oxide from upper and lower surfaces of the semiconductor wafer;

loading the wafer onto a susceptor, wherein a lower surface of the wafer is supported upon the susceptor; and

depositing a layer on the wafer upper surface while the wafer is supported upon the susceptor.

36. The method of claim 35, wherein conducting the native oxide clean and depositing the layer are conducted in situ within a single process chamber.

37. The method of claim 35, wherein conducting the native oxide clean comprises supporting the wafer upon an upper platform vertically spaced above the susceptor.